QL7180 DSP Data Sheet

Combining Embedded DSP Blocks, Performance, Density and Embedded RAM

1.0 Device Highlights

Clock Network

- 9 global clock networks
- 1 dedicated, 8 programmable
- 16 I/O (high drive) networks: 2 banks per I/O
- 20 Quad-net networks: 5 per quadrant

Programmable I/O

- High performance enhanced I/O: less than 3 ns Tco
- Programmable slew rate control
- Programmable I/O standards
- LVTTL, LVCMOS, PCI, GTL+, SSTL2, and SSTL3
- 8 independent I/O banks
- 3 register configuration: Input, Output, OE

Parameterized IP

- Free parameterized IP administered with a DSP Wizard
- Supports multiple and hierarchical IP instantiations

Applications

- Signal processing operators
- Signal processing functions
- Networking / communications for VoIP
- Speech / voice processing
- Channel coding

High Speed Customizable Logic

- 0.25u, 5 layer metal CMOS process
- 2.5 V Vcc, 2.5 / 3.3 V drive capable I/O
- 512 programmable I/O
- 4,032 Logic Cells
- 660,000 max system gates
- Muxed based architecture, non-volatile technology
- Completely customizable for any digital applications

Dual Port SRAM

- 36 blocks of dual-port SRAM
- 2,304 bit dual port high performance SRAM Blocks
- Total of 82,900 bits
- RAM / ROM / FIFO Wizard for automatic configuration
- Configurable and cascadable
- Array sizes of 2, 4, 9, and 18
- < 3 ns access times, 300+ MHz FIFO

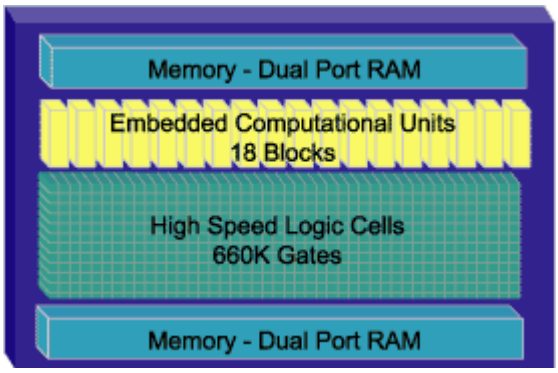

Figure 1: Embedded QuickDSP Block Diagram

2.0 AC Characteristics at Vcc = 2.5V, TA=25° C (K=1.00)

The AC Specifications, Logic Cell diagrams and waveforms are provided below.

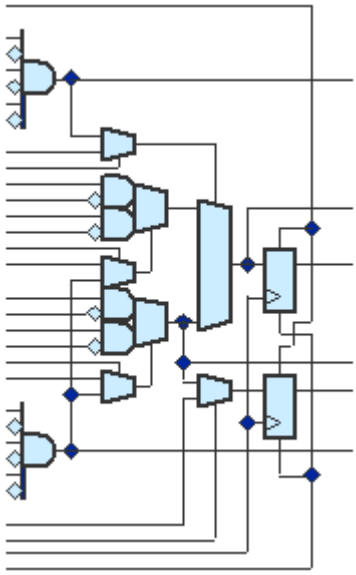

Figure 2: QuickDSP Logic Cell

Table 1: Logic Cells

Symbol	Parameter	Propagation delay (ns)
Logic Cells		**1**
tPD	Combinatorial delay: time taken by the combinatorial circuit to output	0.257
tSU	Setup time: the amount of time the synchronous input of the flip flop must be stable before the active clock edge	0.22
thl	Hold time: the amount of time the synchronous input of the flip flop must be stable after the active block edge	0
tCLK	Clock to out delay: the amount of time the synchronous input of the flip flop must be stable after the active block edge	0.255
tCWHI	Clock High Time: the length of time that the clock stays high	0.46
tCWLO	Clock Low Time: the length of time that the clock stays low	0.46
tSET	Set Delay: amount of time between when the flip flop is ”set” (high) and when Q is consequent “set” (high)	0.18
tRESET	Reset Delay: amount of time between when the flip flop is ”reset” (low) and when Q is consequent “reset” (low)	0.09
tSW	Set Width: length of time that the SET signal remains high (low if active low)	0.3
tRW	Reset Width: length of time that the RESET signal remains high (low if active low)	0.3

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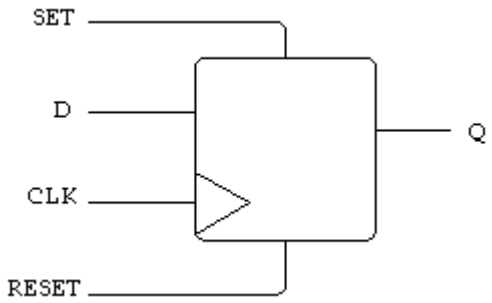

Figure 3: Logic Cell Flip Flop

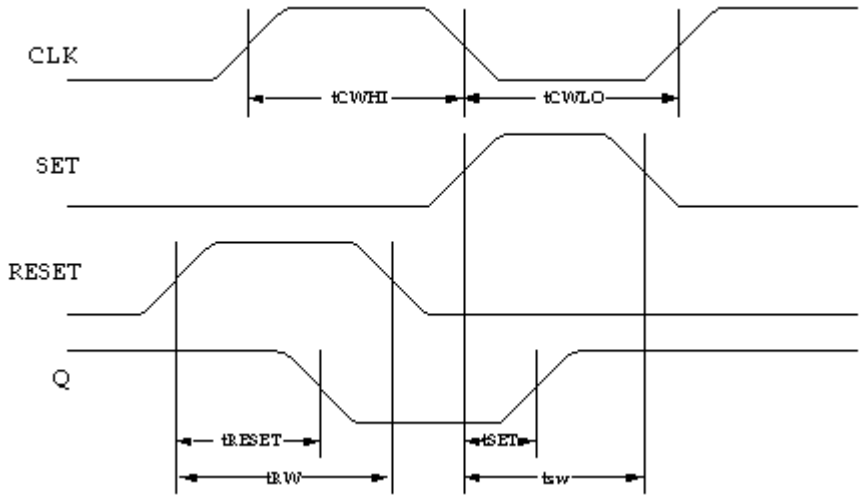

Figure 4: Logic Cell Flip Flop Timings - First Waveform

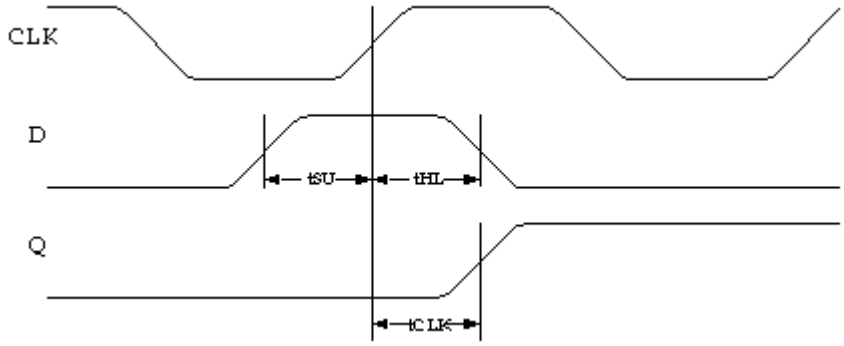

Figure 5: Logic Cell Flip Flop Timings - Second Waveform

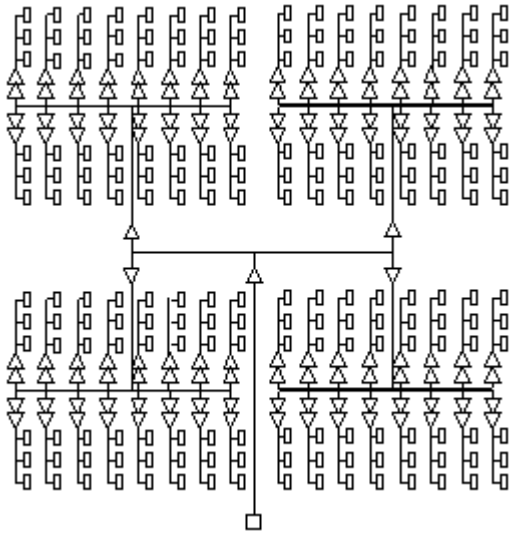

Figure 6: QuickDSP Global Clock Structure

Table 2: QuickDSP Clock Performance

	Clock Performance	
	Global	Dedicated
Macro	1.51 ns	1.59 ns
I/O	2.06 ns	1.73 ns
Skew	0.55 ns	0.14 ns

Table 3: QuickDSP Input Register Cell

Symbol Input Register Cell Only	Parameter	Propagation delay (ns)
tGCKP	Global clock pin delay	
GCKB	Global clock buffer delay	

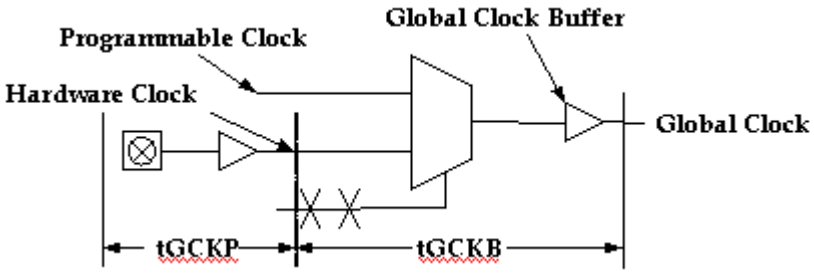

Figure 7: Global Clock Structure Schematic

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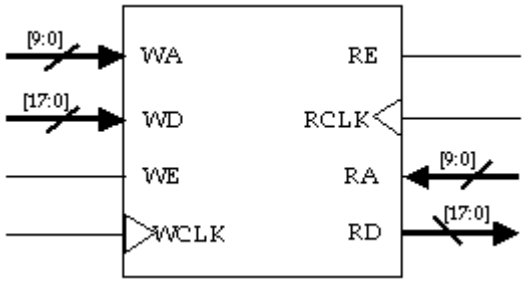

Figure 8: QuickRAM Module

Table 4: RAM Cell Synchronous Write Timing

Symbol	Parameter	Propagation delay (ns)
RAM Cell Synchronous Write Timing		**1**
TSWA	WA Setup Time to WCLK: the amount of time the WRITE ADDRESS must be stable before the active edge of the WRITE CLOCK	0.675
THWA	WA Hold Time to WCLK: the amount of time the WRITE ADDRESS must be stable after the active edge of the WRITE CLOCK	0
TSWD	WD Setup Time to WCLK: the amount of time the WRITE DATA must be stable before the active edge of the WRITE CLOCK	0.654
THWD	WD Hold Time to WCLK: the amount of time the WRITE DATA must be stable after the active edge of the WRITE CLOCK	0
TSWE	WE Setup Time to WCLK: the amount of time the WRITE ENABLE must be stable before the active edge of the WRITE CLOCK	0.623
THWE	WE Hold Time to WCLK: the amount of time the WRITE ENABLE must be stable after the active edge of the WRITE CLOCK	0
TWCRD	WCLK to RD (WA=RA) [5]: the amount of time between the active WRITE CLOCK edge and the time when the data is available at RD	4.38

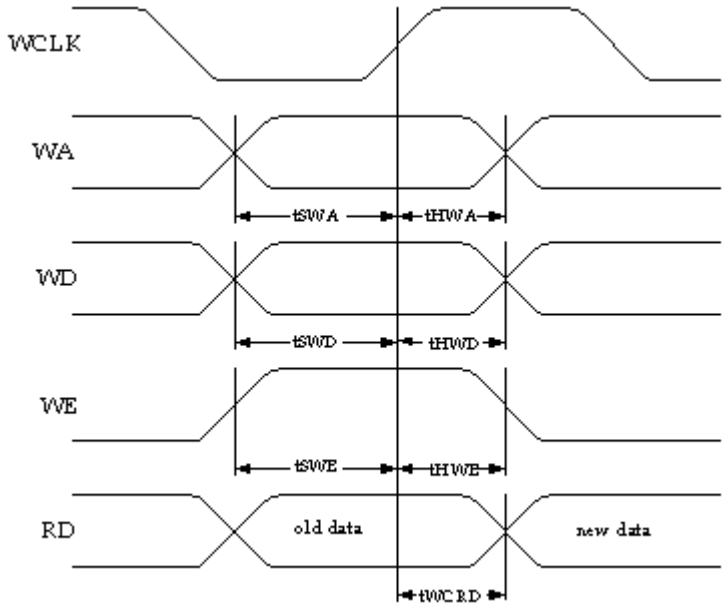

Figure 9: RAM Cell Synchronous Write Timing

Table 5: RAM Cell Synchronous & Asynchronous Read Timing

Symbol	Parameter	Propagation delay (ns)
RAM Cell Synchronous Read Timing		**1**
TSRA	RA Setup Time to RCLK: the amount of time the READ ADDRESS must be stable before the active edge of the READ CLOCK	0.686
THRA	RA Hold Time to RCLK: the amount of time the READ ADDRESS must be stable after the active edge of the READ CLOCK	0
TSRE	RE Setup Time to RCLK: the amount of time the READ ENABLE must be stable before the active edge of the READ CLOCK	0.243
THRE	RE Hold Time to RCLK: the amount of time the READ ENABLE must be stable after the active edge of the READ CLOCK	0
TRCRD	RCLK to RD [5]: the amount of time between the active READ CLOCK edge and the time when the data is available at RD	4.38
RAM Cell Synchronous Read Timing		
RPDRD	RA to RD [5]: amount of time between when the READ ADDRESS is input and when the DATA is output	2.06

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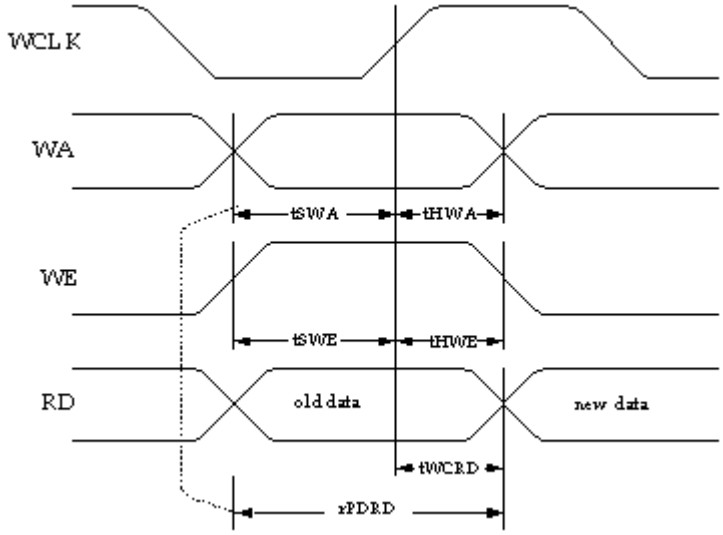

Figure 10: RAM Cell Synchronous & Asynchronous Read Timing

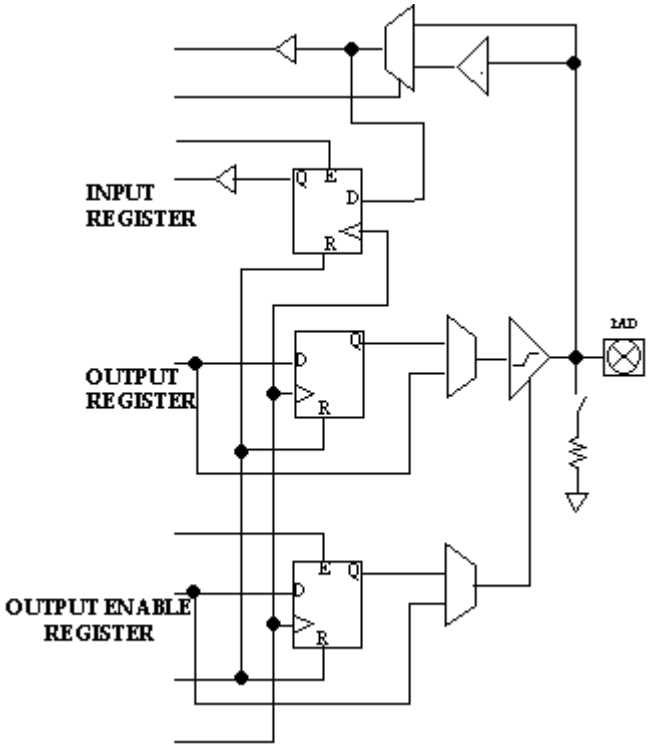

Figure 11: QuickDSP Cell I/O

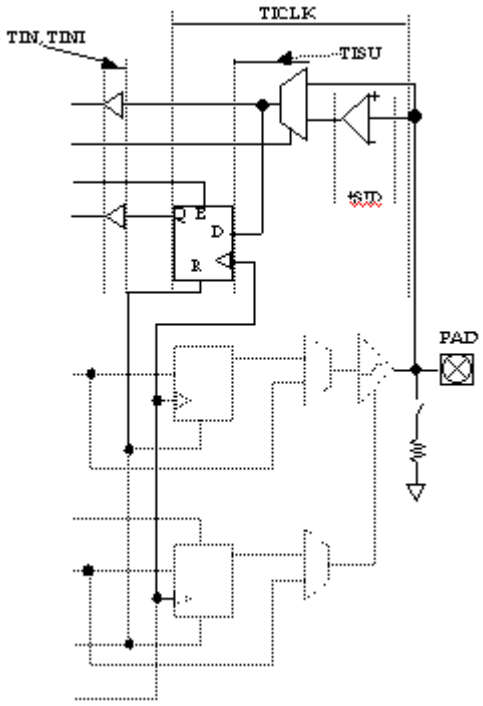

Figure 12: QuickDSP Input Register Cell

Table 6: Input Register Cell

Symbol	Parameter	Propagation delay (ns)
Input Register Cell Only		**1**
tISU	Input register setup time: the amount of time the synchronous input of the flip flop must be stable before the active clock edge	3.12
tIH	Input register hold time: the amount of time the synchronous input of the flip flop must be stable after the active clock edge	0
tICLK	Input register clock to Q: the amount of time taken by the flip flop to output after the active clock edge	1.08
tIRST	Input register reset delay: amount of time between when the flip flop is “reset”(low) and when Q is consequently “reset” (low)	0.99
tIESU	Input register clock enable setup time: the amount of time “enable” must be stable before the active clock edge	0.37
tIEH	Input register clock enable time: the amount of time “enable” must be stable after the active clock edge	0

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Table 7: Standard Input Delays

Symbol Standard Input Delays	Parameter To get the total input delay and this delay to tISU	Propagation delay (ns) 1
tSID (LVTTL)	LVTTL input delay: Low Voltage TTL for 3.3V applications	0.34
tSID (LVCMOS2)	LVCMOS2 input delay: Low Voltage CMOS for 2.5V and lower applications	0.42
tSID (GTL+)	GTL+ input delay: Gunning Transceiver Logic	0.68
tSID (SSTL3)	SSTL3 input delay: Stub Series Terminated Logic for 3.3V	0.55
tSID (SSTL2)	SSTL2 input delay: Stub Series Terminated Logic for 2.5V	0.607

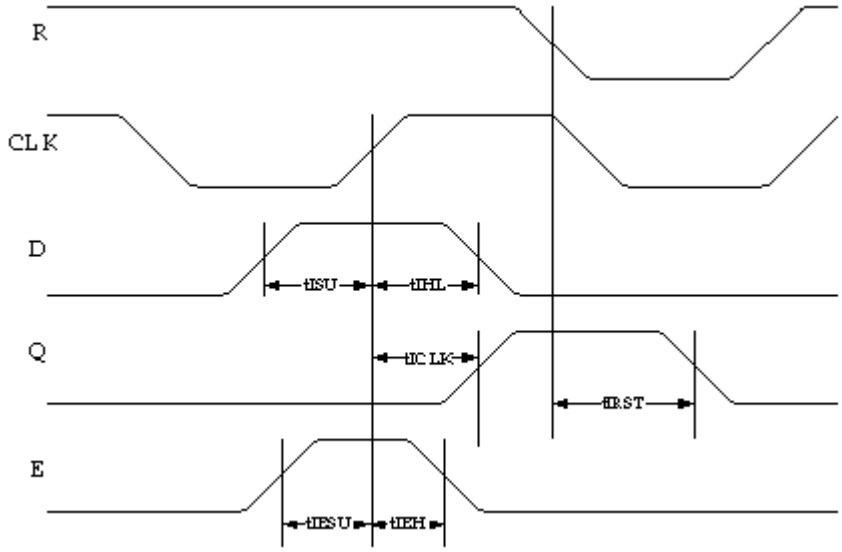

Figure 13: QuickDSP Input Register Cell Timing

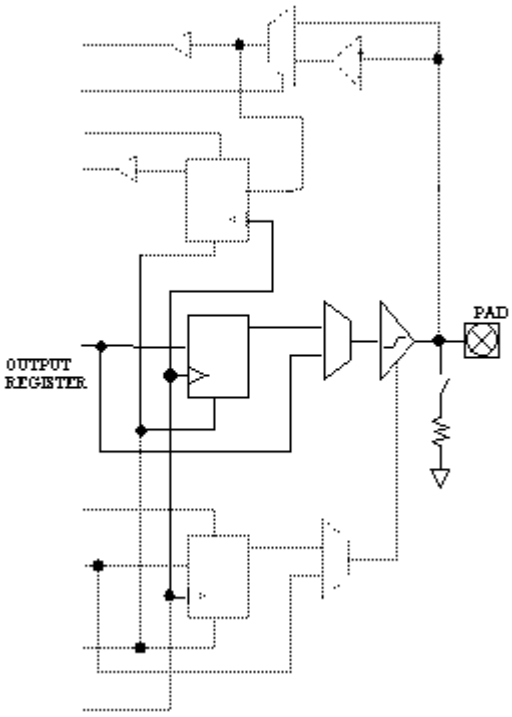

Figure 14: QuickDSP Output Register Cell

Table 8: QuickDSP Output Register Cell

Symbol	Parameter	Propagation delay (ns)
Output Register Cell Only		**1**
TOUTLH	Output Delay Low to High (10% of H)	0.40
TOUTHL	Output Delay High to Low (90% of H)	0.55
TPZH	Output Delay Tri-state to High (10% of Z)	
TPZL	Output Delay Tri-state to Low (90% of Z)	
TPHZ	Output Delay High to Tri-State	3.07
TPLZ	Output Delay Low to Tri-State	2.53

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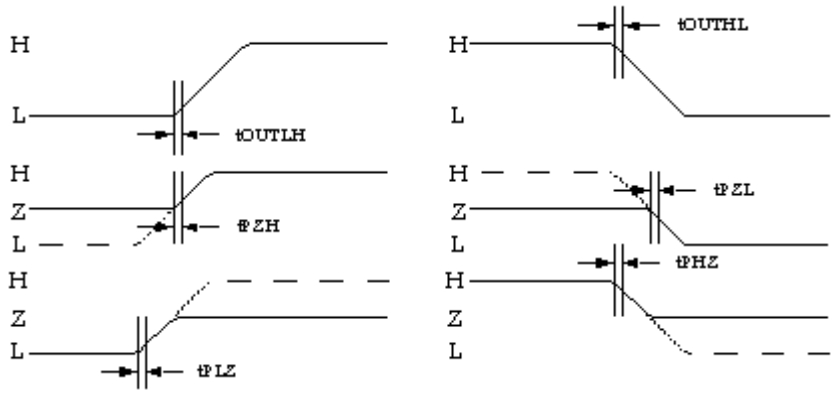

Figure 15: QuickDSP Output Register Cell Timing

Table 9: VCCIO = 3.3 V

	Fast Slew	Slow Slew
Rising Edge	2.8 V/ns	1.0 V/ns
Falling Edge	2.86 V/ns	1.0 V/ns

Table 10: VCCIO = 2.5 V

	Fast Slew	Slow Slew
Rising Edge	1.7 V/ns	0.6 V/ns
Falling Edge	1.9 V/ns	0.6 V/ns

3.0 DC Characteristics

The DC Specifications are provided in the tables below.

Table 11: Absolute Maximum Ratings

V_{CC} Voltage	-0.5 to 3.6V	**DC Input Current**	±20 mA
V_{CCIO} Voltage	-0.5 to 4.6V	**ESD Pad Protection**	±2000V
V_{REF} Voltage	2.7V	**Storage Temperature**	-65°C to +150°C
Input Voltage	-0.5V to V_{CCIO} +0.5V	**Maximum Lead Temperature**	300°C
Latch-up Immunity	±100 mA		

Table 12: Operating Range

Symbol	Parameter		Military		Industrial		Commercial		Unit
			Min	Max	Min	Max	Min	Max	
VCC	Supply Voltage		2.3	2.7	2.3	2.7	2.3	2.7	V
VCCIO	I/O Input Tolerance Voltage		2.3	3.6	2.3	3.6	2.3	3.6	V
TA	Ambient Temperature		-55		-40	85	0	70	°C
TC	Case Temperature			125					°C
K	Delay Factor	-4 Speed Grade	0.42	2.3	0.43	2.16	0.47	2.11	n/a
		-5 Speed Grade	0.42	1.92	0.43	1.80	0.46	1.76	n/a
		-6 Speed Grade	0.42	1.35	0.43	1.26	0.46	1.23	n/a
		-7 Speed Grade	0.42	1.22	0.43	1.14	0.46	1.11	n/a

Table 13: DC Input and Output Levels

	V_{REF}		V_{IL}		V_{IH}		V_{OL}	V_{OH}	I_{OL}	I_{OH}
	V_{MIN}	V_{MAX}	V_{MIN}	V_{MAX}	V_{MIN}	V_{MAX}	V_{MAX}	V_{MIN}	mA	mA
LVTTL	n/a	n/a	-0.3	0.8	2.0	V_{CCIO}-0.3	0.4	24.	2.0	-2.0
LVCMOS2	n/a	n/a	-0.3	0.7	1.7	V_{CCIO}-0.3	0.7	1.7	2.0	-2.0
GTL+	0.88	1.12	-0.3	V_{REF}-2.0	V_{REF}+2.0	V_{CCIO}-0.3	0.6	n/a	40	n/a
PCI	n/a	n/a	-0.3	0.3xV_{CC}	0.5xV_{CC}	V_{CCIO}-0.5	0.1xV_{CC}	0.9xV_C	1.5	-0.5
SSTL2	1.15	1.35	-0.3	V_{REF}-0.18	V_{REF}+0.18	V_{CCIO}+0.3	0.74	1.76	7.6	-7.6
SSTL3	1.3	1.7	-0.3	V_{REF}-0.2	V_{REF}+2.0	V_{CCIO}+0.3	1.10	1.90	9	-8

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4.0 Pin Descriptions

Table 14: Pin Descriptions

Pin	Function	Description
TDI/RSI	Test Data In for JTAG /RAM init. Serial Data In	Hold HIGH during normal operation. Connects to serial PROM data in for RAM initialization. Connect to VCC if unused
TRSTB/RRO	Active low Reset for JTAG /RAM init. reset out	Hold LOW during normal operation. Connects to serial PROM reset for RAM initialization. Connect to GND if unused
TMS	Test Mode Select for JTAG	Hold HIGH during normal operation. Connect to VCC if not used for JTAG
TCK	Test Clock for JTAG	Hold HIGH or LOW during normal operation. Connect to VCC or ground if not used for JTAG
TDO/RCO	Test data out for JTAG /RAM init. clock out	Connect to serial PROM clock for RAM initialization. Must be left unconnected if not used for JTAG or RAM initialization
I/GCLK	High-drive input and/or global network driver	Can be configured as either or both
I/O	Input/Output pin	Can be configured as an input and/or output
VCC	Power supply pin	Connect to 2.5V supply
VCCIO	Input voltage tolerance pin	Connect to 3.3 volt supply if 3.3 volt input tolerance is required, otherwise connect to 2.5V supply
GND	Ground pin	Connect to ground
PLLIN	PLL clock input	Clock input for PLL
DEDCLK	Dedicated clock pin	Low skew global clock
GNDPLL	Ground pin for PLL	Connect to GND
INREF	Differential reference voltage	Connect to reference voltage or ground if used for non-differential input
PLLOUT	PLL output pin	Dedicated PLL output pin. Otherwise may be left unconnected
IOCTRL	Highdrive input	Can be used as highdrive input or clock to I/O register within the same bank. Tied low or high if unused

4.1 Recommended Unused Pin Terminations for the QuickDSP devices

All unused, general purpose I/O pins can be tied to VCC, GND or HIZ (high impedance) internally using the Configuration Editor. The option is given in the right-bottom corner of the Configuration window. The use the Configuration Editor go to: TOOLS/CONFIGURATION PINS.

The rest of the pins should be terminated at the board level in the following manner:

Table 15: Recommended Unused Pin Terminations

Signal Name	Recommended Termination
PLLOUT<x>	Unused PLL output pins must be connected to either VCC or GND so that their associated input buffer never floats. Utilized PLL output pins that route the PLL clock outside of the chip, do not need to be tied to either VCC or GND.
IOCTRL<y>	Any unused pins of this type must be connected to either VCC or GND.
CLK/PLLIN<x>	Any unused clock pins should be connected to VCC or GND.
PLLRST<x>	If a PLL module is not used, then the associated PLLRST<x> must be connected to VCC, under normal operation use it as needed.
INREF<y>	If an I/O bank does not require the use of INREF signal the pin should be connected to GND.

NOTE: *x -> number, y -> alphabetical character*

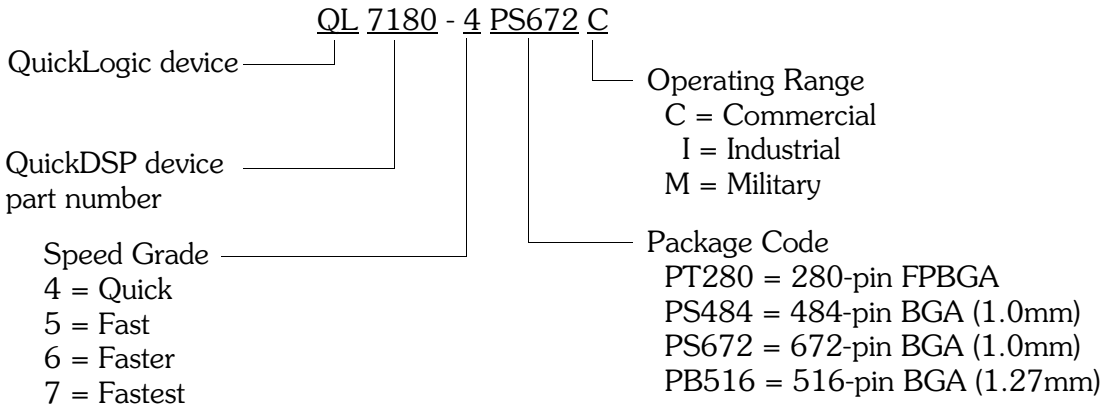

Figure 16: Ordering Information

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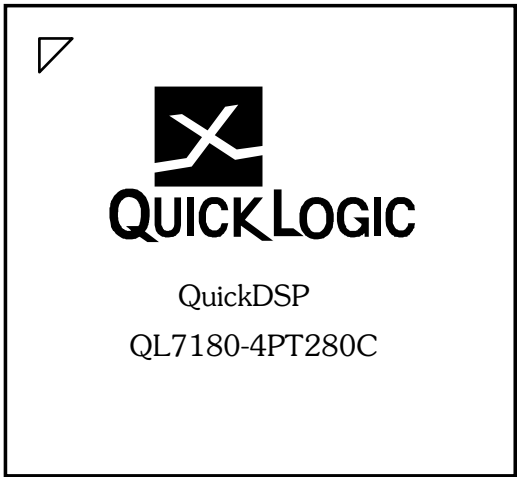
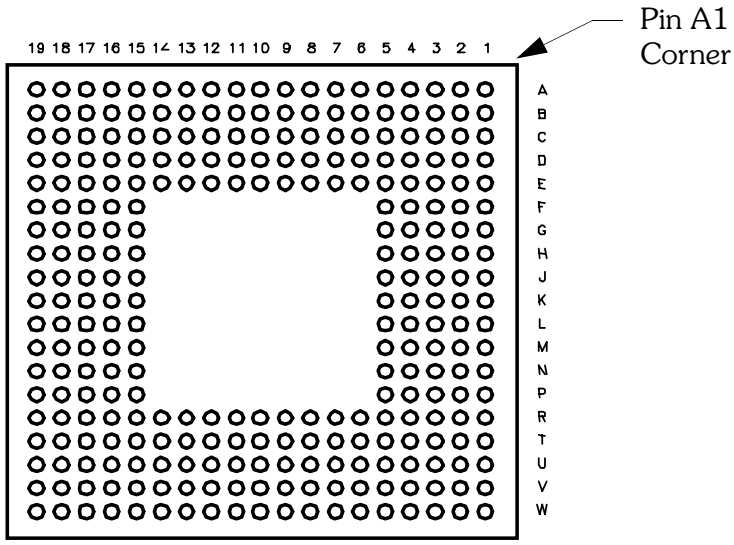
5.0 280 PBGA Pinout Diagram

Top



Bottom



6.0 280 PBGA Pinout Table

Table 16: 280 PBGA Pinout Table

280 PBGA	Function	280 PBGA	Function	280 PBGA	Function	280 PBGA	Function	280 PBGA	Function	280 PBGA	Function
A1	PLLOUT<3>	C10	CLK<5>/PLLIN<3>	E19	IOCTRL<D>	K16	I/O<C>	R4	I/O<H>	U13	I/O<B>
A2	GNDPLL<0>	C11	VCCIO<E>	F1	INREF<G>	K17	I/O<D>	R5	GND	U14	IOCTRL<B>
A3	I/O<F>	C12	I/O<E>	F2	IOCTRL<G>	K18	I/O<C>	R6	GND	U15	VCCIO<B>
A4	I/O<F>	C13	I/O<E>	F3	I/O<G>	K19	TRSTB	R7	VCC	U16	I/O<B>
A5	I/O<F>	C14	I/O<E>	F4	I/O<G>	L1	I/O<H>	R8	VCC	U17	TDO
A6	IOCTRL<F>	C15	VCCIO<E>	F5	GND	L2	I/O<H>	R9	GND	U18	PLLRST<2>
A7	I/O<F>	C16	I/O<E>	F15	VCC	L3	VCCIO<H>	R10	GND	U19	I/O<B>
A8	I/O<F>	C17	I/O<E>	F16	IOCTRL<D>	L4	I/O<H>	R11	VCC	V1	PLLOUT<2>
A9	I/O<F>	C18	I/O<E>	F17	I/O<D>	L5	VCC	R12	VCC	V2	GNDPLL<3>
A10	CLK<7>	C19	I/O<E>	F18	I/O<D>	L15	GND	R13	VCC	V3	GND
A11	I/O<E>	D1	I/O<G>	F19	I/O<D>	L16	I/O<C>	R14	VCC	V4	I/O<A>
A12	I/O<E>	D2	I/O<G>	G1	I/O<G>	L17	VCCIO<C>	R15	GND	V5	I/O<A>
A13	I/O<E>	D3	I/O<F>	G2	I/O<G>	L18	I/O<C>	R16	I/O<C>	V6	IOCTRL<A>
A14	IOCTRL<E>	D4	I/O<F>	G3	IOCTRL<G>	L19	I/O<C>	R17	VCCIO<C>	V7	I/O<A>
A15	I/O<E>	D5	I/O<F>	G4	I/O<G>	M1	I/O<H>	R18	I/O<C>	V8	I/O<A>
A16	I/O<E>	D6	I/O<F>	G5	VCC	M2	I/O<H>	R19	I/O<C>	V9	I/O<A>
A17	I/O<E>	D7	I/O<F>	G15	VCC	M3	I/O<H>	T1	I/O<H>	V10	CLK<1>
A18	PLLRST<1>	D8	I/O<F>	G16	I/O<D>	M4	I/O<H>	T2	I/O<H>	V11	CLK<4>DEDCLK/PLLIN<0>
A19	GND	D9	CLK<8>	G17	I/O<D>	M5	VCC	T3	I/O<A>	V12	I/O<B>
B1	PLLRST<0>	D10	I/O<E>	G18	I/O<D>	M15	VCC	T4	I/O<A>	V13	I/O<B>
B2	GND	D11	I/O<E>	G19	I/O<D>	M16	INREF<C>	T5	I/O<A>	V14	INREF<B>
B3	I/O<F>	D12	I/O<E>	H1	I/O<G>	M17	I/O<C>	T6	IOCTRL<A>	V15	I/O<B>
B4	I/O<F>	D13	INREF<E>	H2	I/O<G>	M18	I/O<C>	T7	I/O<A>	V16	I/O<B>
B5	I/O<F>	D14	I/O<E>	H3	I/O<G>	M19	I/O<C>	T8	I/O<A>	V17	I/O<B>
B6	INREF<F>	D15	I/O<E>	H4	I/O<G>	N1	IOCTRL<H>	T9	I/O<A>	V18	GNDPLL<2>
B7	I/O<F>	D16	I/O<D>	H5	VCC	N2	I/O<H>	T10	I/O<A>	V19	GND
B8	I/O<F>	D17	I/O<D>	H15	VCC	N3	I/O<H>	T11	CLK<3>/PLLIN<1>	W1	GND
B9	TMS	D18	I/O<D>	H16	VCC	N4	I/O<H>	T12	I/O<B>	W2	PLLRST<3>
B10	CLK<6>	D19	I/O<D>	H17	I/O<D>	N5	VCC	T13	I/O<B>	W3	I/O<A>
B11	I/O<E>	E1	I/O<G>	H18	I/O<D>	N15	VCC	T14	I/O<B>	W4	I/O<A>
B12	I/O<E>	E2	I/O<G>	H19	I/O<D>	N16	I/O<C>	T15	I/O<B>	W5	I/O<A>
B13	IOCTRL<E>	E3	VCCIO<G>	J1	I/O<G>	N17	I/O<C>	T16	I/O<B>	W6	I/O<A>
B14	I/O<E>	E4	I/O<F>	J2	I/O<G>	N18	IOCTRL<C>	T17	VCCPLL<2>	W7	I/O<A>
B15	I/O<E>	E5	GND	J3	VCCIO<G>	N19	IOCTRL<C>	T18	I/O<B>	W8	I/O<A>
B16	I/O<E>	E6	VCC	J4	I/O<G>	P1	I/O<H>	T19	I/O<B>	W9	TDI
B17	VCCPLL<1>	E7	VCC	J5	GND	P2	I/O<H>	U1	I/O<A>	W10	CLK<2>/PLLIN<2>
B18	GNDPLL<1>	E8	VCC	J15	VCC	P3	IOCTRL<H>	U2	I/O<A>	W11	I/O<B>
B19	PLLOUT<0>	E9	VCC	J16	I/O<C>	P4	INREF<H>	U3	VCCPLL<3>	W12	I/O<B>
C1	I/O<F>	E10	GND	J17	VCCIO<D>	P5	VCC	U4	I/O<A>	W13	I/O<B>
C2	VCCPLL<0>	E11	GND	J18	I/O<D>	P15	GND	U5	VCCIO<A>	W14	IOCTRL<B>
C3	I/O<F>	E12	VCC	J19	I/O<D>	P16	I/O<C>	U6	INREF<A>	W15	I/O<B>
C4	I/O<F>	E13	VCC	K1	VCC	P17	I/O<C>	U7	I/O<A>	W16	I/O<B>
C5	VCCIO<F>	E14	GND	K2	TCK	P18	I/O<C>	U8	I/O<A>	W17	I/O<B>
C6	IOCTRL<F>	E15	GND	K3	I/O<G>	P19	I/O<C>	U9	VCCIO<A>	W18	I/O<B>
C7	I/O<F>	E16	I/O<D>	K4	I/O<G>	R1	I/O<H>	U10	CLK<0>	W19	PLLOUT<1>
C8	I/O<F>	E17	VCCIO<D>	K5	GND	R2	I/O<H>	U11	VCCIO<B>		
C9	VCCIO<F>	E18	INREF<D>	K15	GND	R3	VCCIO<H>	U12	I/O<B>		

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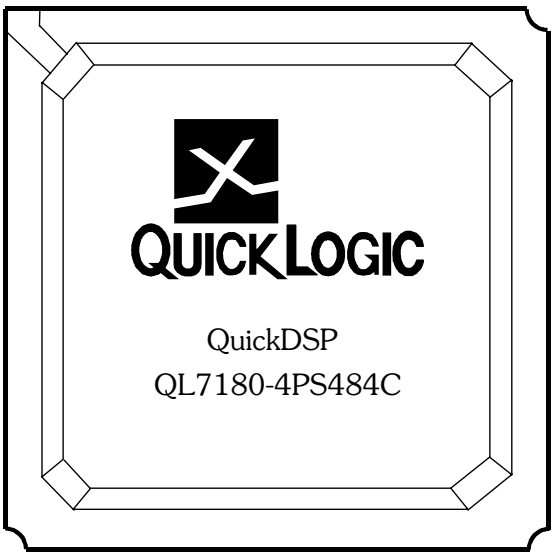
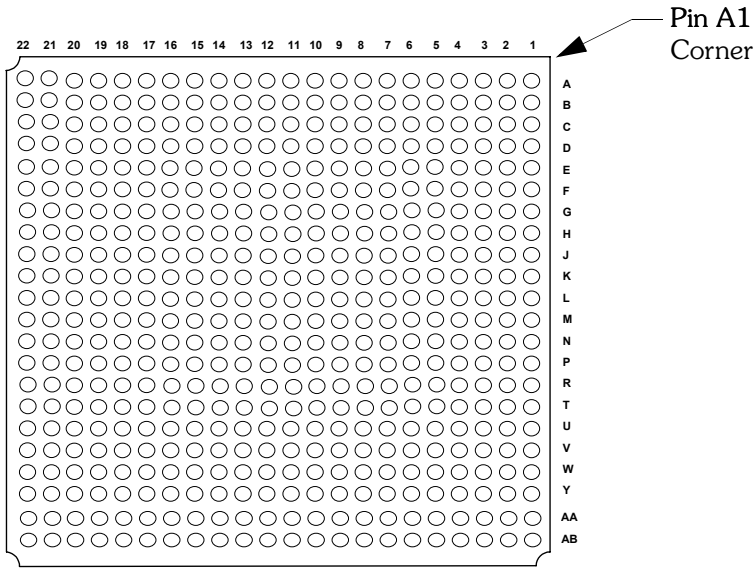
7.0 484 PBGA Pinout Diagram

Top



Bottom



8.0 484 PBGA Pinout Table

Table 17: 484 PBGA Pinout Table

484 PBGA	Function	484 PBGA	Function	484 PBGA	Function	484 PBGA	Function	484 PBGA	Function	484 PBGA	Function
A1	I/O<A>	C18	I/O<G>	F13	I/O<G>	J8	VCC	M3	I/O<B>	P20	I/O<E>
A2	PLLRST<3>	C19	I/O<F>	F14	VCCIO<G>	J9	GND	M4	CLK<3>/PLLIN<1>	P21	I/O<E>
A3	I/O<A>	C20	GNDPLL<0>	F15	I/O<G>	J10	VCC	M5	I/O<B>	P22	I/O<E>
A4	I/O<A>	C21	I/O<F>	F16	VCCIO<G>	J11	VCC	M6	VCCIO<B>	R1	I/O<B>
A5	I/O<A>	C22	I/O<F>	F17	I/O<G>	J12	GND	M7	CLK<1>	R2	INREF<B>
A6	I/O<H>	D1	I/O<A>	F18	I/O<F>	J13	VCC	M8	VCC	R3	I/O<B>
A7	I/O<H>	D2	I/O<A>	F19	I/O<F>	J14	GND	M9	VCC	R4	I/O<B>
A8	IOCTRL<H>	D3	I/O<A>	F20	IOCTRL<F>	J15	VCC	M10	GND	R5	I/O<B>
A9	I/O<H>	D4	I/O<A>	F21	I/O<F>	J16	I/O<F>	M11	GND	R6	I/O<B>
A10	I/O<H>	D5	I/O<A>	F22	IOCTRL<F>	J17	VCCIO<F>	M12	GND	R7	I/O<B>
A11	I/O<H>	D6	I/O<H>	G1	I/O<A>	J18	I/O<F>	M13	GND	R8	GND
A12	TCK	D7	I/O<H>	G2	I/O<A>	J19	I/O<F>	M14	GND	R9	VCC
A13	I/O<G>	D8	I/O<H>	G3	I/O<A>	J20	I/O<F>	M15	GND	R10	VCC
A14	I/O<G>	D9	I/O<H>	G4	I/O<A>	J21	I/O<F>	M16	GND	R11	GND
A15	I/O<G>	D10	I/O<H>	G5	I/O<A>	J22	I/O<F>	M17	I/O<E>	R12	VCC
A16	I/O<G>	D11	I/O<H>	G6	I/O<A>	K1	TDI	M18	I/O<E>	R13	VCC
A17	I/O<G>	D12	I/O<G>	G7	GND	K2	I/O<A>	M19	I/O<E>	R14	VCC
A18	I/O<G>	D13	I/O<G>	G8	I/O<H>	K3	I/O<A>	M20	CLK<7>	R15	GND
A19	I/O<F>	D14	I/O<G>	G9	I/O<H>	K4	I/O<A>	M21	CLK<5>/PLLIN<3>	R16	I/O<D>
A20	GND	D15	IOCTRL<G>	G10	I/O<H>	K5	I/O<A>	M22	TMS	R17	VCCIO<E>
A21	PLLOUT<3>	D16	I/O<G>	G11	I/O<G>	K6	VCCIO<A>	N1	I/O<B>	R18	I/O<E>
A22	I/O<F>	D17	I/O<G>	G12	GND	K7	I/O<A>	N2	I/O<B>	R19	I/O<E>
B1	I/O<A>	D18	I/O<F>	G13	I/O<G>	K8	VCC	N3	I/O<B>	R20	I/O<E>
B2	GND	D19	VCCPLL<0>	G14	I/O<G>	K9	VCC	N4	I/O<B>	R21	I/O<E>
B3	GNDPLL<3>	D20	I/O<F>	G15	I/O<G>	K10	GND	N5	I/O<B>	R22	I/O<E>
B4	GND	D21	I/O<F>	G16	GND	K11	GND	N6	I/O<B>	T1	I/O<B>
B5	I/O<A>	D22	I/O<F>	G17	VCCIO<F>	K12	GND	N7	I/O<B>	T2	I/O<B>
B6	I/O<H>	E1	IOCTRL<A>	G18	I/O<F>	K13	GND	N8	VCC	T3	I/O<B>
B7	I/O<H>	E2	I/O<A>	G19	I/O<F>	K14	VCC	N9	VCC	T4	I/O<B>
B8	INREF<H>	E3	I/O<A>	G20	I/O<F>	K15	VCC	N10	GND	T5	I/O<B>
B9	I/O<H>	E4	I/O<A>	G21	INREF<F>	K16	I/O<F>	N11	GND	T6	VCCIO<B>
B10	I/O<H>	E5	I/O<A>	G22	I/O<F>	K17	I/O<F>	N12	GND	T7	GND
B11	I/O<H>	E6	I/O<H>	H1	I/O<A>	K18	I/O<F>	N13	GND	T8	I/O<C>
B12	I/O<G>	E7	I/O<H>	H2	I/O<A>	K19	I/O<F>	N14	VCC	T9	I/O<C>
B13	I/O<G>	E8	I/O<H>	H3	I/O<A>	K20	I/O<F>	N15	VCC	T10	TRSTB
B14	I/O<G>	E9	I/O<H>	H4	I/O<A>	K21	I/O<F>	N16	I/O<E>	T11	GND
B15	I/O<G>	E10	I/O<H>	H5	IOCTRL<A>	K22	I/O<F>	N17	VCCIO<E>	T12	I/O<C>
B16	I/O<G>	E11	VCC	H6	VCCIO<A>	L1	CLK<4> DEDCLK/PLLIN<0>	N18	I/O<E>	T13	I/O<D>
B17	I/O<G>	E12	I/O<G>	H7	I/O<H>	L2	CLK<0>	N19	I/O<E>	T14	I/O<D>
B18	I/O<G>	E13	I/O<G>	H8	GND	L3	CLK<2>/PLLIN<2>	N20	I/O<E>	T15	I/O<D>
B19	PLLRST<0>	E14	I/O<G>	H9	VCC	L4	I/O<A>	N21	I/O<E>	T16	GND
B20	I/O<F>	E15	IOCTRL<G>	H10	VCC	L5	I/O<A>	N22	I/O<E>	T17	I/O<E>
B21	I/O<F>	E16	I/O<G>	H11	VCC	L6	I/O<A>	P1	I/O<B>	T18	I/O<E>
B22	I/O<F>	E17	INREF<G>	H12	GND	L7	GND	P2	I/O<B>	T19	I/O<E>
C1	I/O<A>	E18	I/O<G>	H13	VCC	L8	GND	P3	I/O<B>	T20	I/O<E>
C2	I/O<A>	E19	I/O<F>	H14	VCC	L9	GND	P4	I/O<B>	T21	IOCTRL<E>
C3	VCCPLL<3>	E20	I/O<F>	H15	GND	L10	GND	P5	I/O<B>	T22	I/O<E>
C4	PLLOUT<2>	E21	I/O<F>	H16	I/O<F>	L11	GND	P6	VCCIO<B>	U1	IOCTRL<B>
C5	I/O<A>	E22	I/O<F>	H17	I/O<F>	L12	GND	P7	I/O<B>	U2	I/O<B>
C6	I/O<H>	F1	I/O<A>	H18	I/O<F>	L13	GND	P8	VCC	U3	IOCTRL<B>
C7	I/O<H>	F2	INREF<A>	H19	I/O<F>	L14	VCC	P9	GND	U4	I/O<B>
C8	I/O<H>	F3	I/O<A>	H20	I/O<F>	L15	VCC	P10	VCC	U5	I/O<B>
C9	IOCTRL<H>	F4	I/O<A>	H21	I/O<F>	L16	CLK<6>	P11	GND	U6	I/O<C>
C10	I/O<H>	F5	I/O<A>	H22	I/O<F>	L17	VCCIO<F>	P12	VCC	U7	VCCIO<C>
C11	I/O<H>	F6	VCCIO<A>	J1	I/O<A>	L18	I/O<F>	P13	VCC	U8	I/O<C>
C12	I/O<H>	F7	VCCIO<H>	J2	I/O<A>	L19	CLK<8>	P14	GND	U9	VCCIO<C>
C13	I/O<G>	F8	I/O<H>	J3	I/O<A>	L20	I/O<F>	P15	VCC	U10	I/O<C>
C14	I/O<G>	F9	VCCIO<H>	J4	I/O<A>	L21	I/O<F>	P16	I/O<E>	U11	VCCIO<C>
C15	I/O<G>	F10	I/O<H>	J5	I/O<A>	L22	I/O<F>	P17	I/O<E>	U12	VCCIO<D>
C16	I/O<G>	F11	VCCIO<H>	J6	I/O<A>	M1	I/O<B>	P18	I/O<E>	U13	I/O<D>

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Table 17: 484 PBGA Pinout Table (Continued)

484 PBGA	Function	484 PBGA	Function	484 PBGA	Function	484 PBGA	Function	484 PBGA	Function	484 PBGA	Function
C17	I/O<G>	F12	VCCIO<G>	J7	I/O<A>	M2	I/O<B>	P19	I/O<E>	U14	VCCIO<D>
U15	I/O<D>	V13	I/O<D>	W11	I/O<C>	Y9	I/O<C>	AA7	I/O<C>	AB5	I/O<B>
U16	VCCIO<D>	V14	I/O<D>	W12	I/O<D>	Y10	I/O<C>	AA8	INREF<C>	AB6	I/O<C>
U17	VCCIO<E>	V15	I/O<D>	W13	I/O<D>	Y11	I/O<D>	AA9	I/O<C>	AB7	I/O<C>
U18	I/O<E>	V16	INREF<D>	W14	I/O<D>	Y12	I/O<D>	AA10	I/O<C>	AB8	IOCTRL<C>
U19	I/O<E>	V17	I/O<D>	W15	I/O<D>	Y13	I/O<D>	AA11	I/O<C>	AB9	I/O<C>
U20	IOCTRL<E>	V18	I/O<E>	W16	I/O<D>	Y14	I/O<D>	AA12	I/O<D>	AB10	I/O<C>
U21	I/O<E>	V19	I/O<E>	W17	I/O<D>	Y15	IOCTRL<D>	AA13	I/O<D>	AB11	I/O<C>
U22	INREF<E>	V20	I/O<E>	W18	I/O<E>	Y16	I/O<D>	AA14	I/O<D>	AB12	I/O<D>
V1	I/O<B>	V21	I/O<E>	W19	I/O<E>	Y17	I/O<D>	AA15	I/O<D>	AB13	I/O<D>
V2	I/O<B>	V22	I/O<E>	W20	I/O<E>	Y18	I/O<E>	AA16	I/O<D>	AB14	I/O<D>
V3	I/O<B>	W1	I/O<B>	W21	I/O<E>	Y19	PLLOUT<0>	AA17	I/O<D>	AB15	I/O<D>
V4	I/O<B>	W2	I/O<B>	W22	I/O<E>	Y20	PLLRST<1>	AA18	I/O<D>	AB16	IOCTRL<D>
V5	I/O<B>	W3	I/O<B>	Y1	I/O<B>	Y21	I/O<E>	AA19	I/O<E>	AB17	I/O<D>
V6	I/O<C>	W4	I/O<B>	Y2	I/O<B>	Y22	I/O<E>	AA20	GNDPLL<1>	AB18	I/O<D>
V7	I/O<C>	W5	I/O<B>	Y3	VCCPLL<2>	AA1	TDO	AA21	I/O<E>	AB19	I/O<E>
V8	I/O<C>	W6	I/O<C>	Y4	I/O<C>	AA2	PLLOUT<1>	AA22	I/O<E>	AB20	GND
V9	I/O<C>	W7	I/O<C>	Y5	I/O<C>	AA3	GND	AB1	I/O<B>	AB21	VCCPLL<1>
V10	I/O<C>	W8	I/O<C>	Y6	I/O<C>	AA4	I/O<B>	AB2	GNDPLL<2>	AB22	I/O<E>
V11	I/O<C>	W9	I/O<C>	Y7	I/O<C>	AA5	I/O<C>	AB3	PLLRST<2>		
V12	VCC	W10	I/O<C>	Y8	IOCTRL<C>	AA6	I/O<C>	AB4	I/O<B>		

9.0 516 PBGA Pinout Diagram

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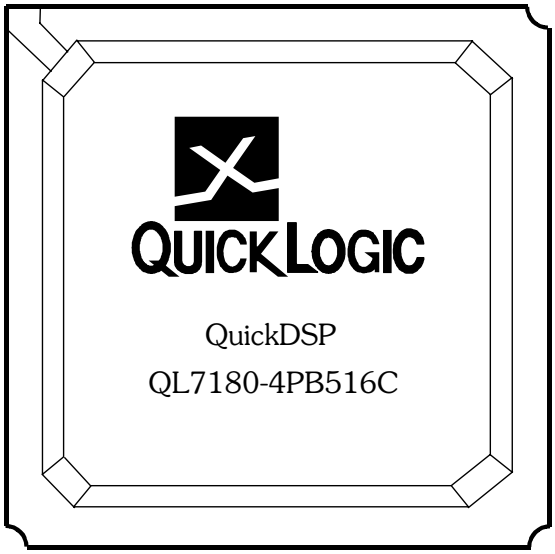
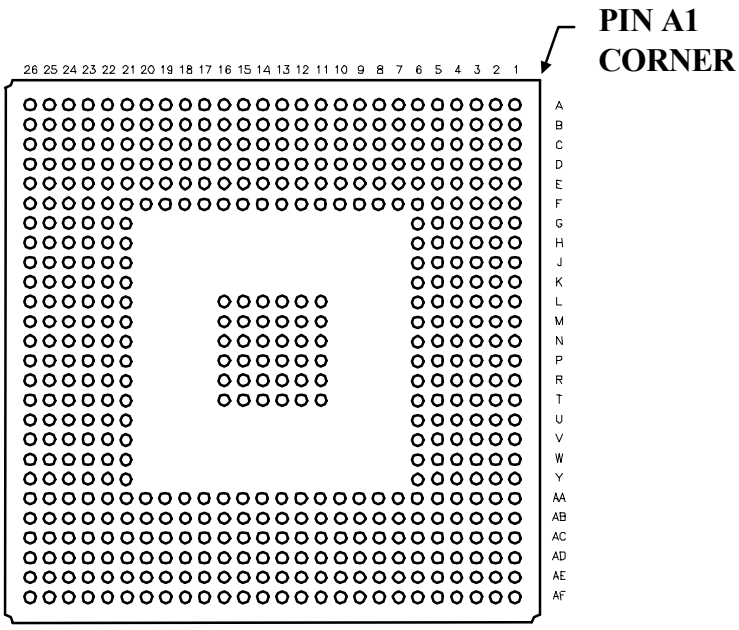


Bottom



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10.0 516 PBGA Pinout Table

Table 18: 516 PBGA Pinout Table

516 PBGA	Function	516 PBGA	Function	516 PBGA	Function	516 PBGA	Function	516 PBGA	Function	516 PBGA	Function
A1	GND	C7	I/O<F>	E13	I/O<F>	H21	VCC	M15	GND	R23	I/O<C>
A2	I/O<F>	C8	INREF<F>	E14	I/O<F>	H22	VCC	M16	GND	R24	I/O<C>
A3	I/O<F>	C9	I/O<F>	E15	I/O<E>	H23	I/O<D>	M21	VCCIO<D>	R25	I/O<C>
A4	I/O<F>	C10	I/O<F>	E16	VCC	H24	IOCTRL<D>	M22	VCC	R26	I/O<C>
A5	I/O<F>	C11	I/O<F>	E17	CLK<6>	H25	IOCTRL<D>	M23	I/O<D>	T1	I/O<H>
A6	I/O<F>	C12	I/O<F>	E18	I/O<E>	H26	I/O<D>	M24	I/O<D>	T2	I/O<H>
A7	IOCTRL<F>	C13	CLK<7>	E19	I/O<E>	J1	I/O<G>	M25	I/O<D>	T3	I/O<H>
A8	I/O<F>	C14	I/O<E>	E20	I/O<E>	J2	I/O<G>	M26	I/O<D>	T4	I/O<H>
A9	I/O<F>	C15	I/O<E>	E21	I/O<E>	J3	I/O<G>	N1	TCK	T5	I/O<H>
A10	I/O<F>	C16	I/O<E>	E22	I/O<E>	J4	I/O<G>	N2	I/O<H>	T6	VCC
A11	I/O<F>	C17	I/O<E>	E23	GNDPLL<1>	J5	I/O<G>	N3	I/O<G>	T11	GND
A12	I/O<F>	C18	I/O<E>	E24	I/O<E>	J6	VCCIO<G>	N4	I/O<G>	T12	GND
A13	I/O<E>	C19	I/O<E>	E25	I/O<D>	J21	VCCIO<D>	N5	I/O<G>	T13	GND
A14	I/O<E>	C20	I/O<E>	E26	I/O<D>	J22	I/O<D>	N6	GND	T14	GND
A15	I/O<E>	C21	I/O<E>	F1	IOCTRL<G>	J23	I/O<D>	N11	GND	T15	GND
A16	I/O<E>	C22	I/O<E>	F2	I/O<G>	J24	I/O<D>	N12	GND	T16	GND
A17	I/O<E>	C23	I/O<E>	F3	I/O<G>	J25	I/O<D>	N13	GND	T21	VCC
A18	IOCTRL<E>	C24	I/O<E>	F4	I/O<G>	J26	I/O<D>	N14	GND	T22	VCC
A19	IOCTRL<E>	C25	I/O<E>	F5	I/O<F>	K1	I/O<G>	N15	GND	T23	I/O<C>
A20	I/O<E>	C26	I/O<E>	F6	GND	K2	I/O<G>	N16	GND	T24	I/O<C>
A21	I/O<E>	D1	I/O<G>	F7	VCCIO<F>	K3	I/O<G>	N21	GND	T25	I/O<C>
A22	I/O<E>	D2	I/O<G>	F8	VCC	K4	I/O<G>	N22	I/O<D>	T26	I/O<C>
A23	I/O<E>	D3	I/O<F>	F9	VCCIO<F>	K5	I/O<G>	N23	I/O<D>	U1	I/O<H>
A24	I/O<E>	D4	I/O<F>	F10	GND	K6	GND	N24	I/O<D>	U2	I/O<H>
A25	PLLRST<1>	D5	GNDPLL<0>	F11	VCC	K21	GND	N25	I/O<D>	U3	I/O<H>
A26	GND	D6	I/O<F>	F12	VCCIO<F>	K22	I/O<D>	N26	I/O<D>	U4	I/O<H>
B1	I/O<F>	D7	I/O<F>	F13	GND	K23	I/O<D>	P1	I/O<H>	U5	I/O<H>
B2	PLLRST<0>	D8	I/O<F>	F14	VCCIO<E>	K24	I/O<D>	P2	I/O<H>	U6	GND
B3	I/O<F>	D9	I/O<F>	F15	VCC	K25	I/O<D>	P3	I/O<H>	U21	GND
B4	I/O<F>	D10	I/O<F>	F16	VCC	K26	I/O<D>	P4	VCC	U22	I/O<C>
B5	I/O<F>	D11	I/O<F>	F17	GND	L1	I/O<G>	P5	I/O<H>	U23	I/O<C>
B6	I/O<F>	D12	I/O<F>	F18	VCCIO<E>	L2	I/O<G>	P6	VCCIO<H>	U24	I/O<C>
B7	IOCTRL<F>	D13	TMS	F19	VCC	L3	I/O<G>	P11	GND	U25	I/O<C>
B8	I/O<F>	D14	I/O<E>	F20	VCCIO<E>	L4	I/O<G>	P12	GND	U26	I/O<C>
B9	I/O<F>	D15	I/O<E>	F21	GND	L5	VCC	P13	GND	V1	I/O<H>
B10	I/O<F>	D16	I/O<F>	F22	I/O<E>	L6	VCC	P14	GND	V2	IOCTRL<H>
B11	I/O<F>	D17	I/O<E>	F23	I/O<D>	L11	GND	P15	GND	V3	IOCTRL<H>
B12	I/O<F>	D18	I/O<F>	F24	I/O<D>	L12	GND	P16	GND	V4	I/O<H>
B13	CLK<5>/PLLIN<3>	D19	CLK<8>	F25	I/O<D>	L13	GND	P21	VCCIO<C>	V5	I/O<H>
B14	I/O<E>	D20	I/O<E>	F26	I/O<D>	L14	GND	P22	I/O<C>	V6	VCCIO<H>
B15	I/O<E>	D21	I/O<E>	G1	I/O<G>	L15	GND	P23	VCC	V21	VCCIO<C>
B16	I/O<E>	D22	I/O<E>	G2	INREF<G>	L16	GND	P24	I/O<C>	V22	I/O<C>
B17	I/O<E>	D23	VCCPLL<1>	G3	I/O<G>	L21	VCC	P25	I/O<C>	V23	I/O<C>
B18	INREF<E>	D24	I/O<E>	G4	I/O<G>	L22	I/O<D>	P26	TRSTB	V24	IOCTRL<C>
B19	I/O<E>	D25	I/O<E>	G5	I/O<G>	L23	I/O<D>	R1	I/O<H>	V25	I/O<C>
B20	I/O<E>	D26	I/O<D>	G6	VCCIO<G>	L24	I/O<D>	R2	I/O<H>	V26	I/O<C>
B21	I/O<E>	E1	I/O<G>	G21	VCCIO<D>	L25	I/O<D>	R3	I/O<H>	W1	INREF<H>
B22	I/O<E>	E2	I/O<G>	G22	I/O<D>	L26	I/O<D>	R4	I/O<H>	W2	I/O<H>
B23	I/O<E>	E3	I/O<G>	G23	I/O<D>	M1	I/O<G>	R5	VCC	W3	I/O<H>
B24	I/O<E>	E4	VCCPLL<0>	G24	I/O<D>	M2	I/O<G>	R6	VCC	W4	I/O<H>
B25	I/O<E>	E5	I/O<F>	G25	I/O<D>	M3	I/O<G>	R11	GND	W5	VCC
B26	PLLOUT<0>	E6	I/O<F>	G26	INREF<D>	M4	I/O<G>	R12	GND	W6	VCC
C1	I/O<F>	E7	I/O<F>	H1	I/O<G>	M5	I/O<G>	R13	GND	W21	VCC
C2	I/O<F>	E8	VCC	H2	I/O<G>	M6	VCCIO<G>	R14	GND	W22	I/O<C>
C3	I/O<F>	E9	I/O<F>	H3	IOCTRL<G>	M11	GND	R15	GND	W23	I/O<C>
C4	PLLOUT<3>	E10	I/O<F>	H4	I/O<G>	M12	GND	R16	GND	W24	I/O<C>
C5	I/O<F>	E11	I/O<F>	H5	I/O<G>	M13	GND	R21	VCC	W25	INREF<C>
C6	I/O<F>	E12	VCC	H6	VCC	M14	GND	R22	I/O<C>	W26	I/O<C>
Y1	I/O<H>	AA17	GND	AB19	VCC	AC21	I/O<B>	AD23	I/O<B>	AE25	PLLRST<2>
Y2	I/O<H>	AA18	VCCIO<B>	AB20	I/O<B>	AC22	TDO	AD24	GND	AE26	I/O<B>

Table 18: 516 PBGA Pinout Table (Continued)

516 PBGA	Function	516 PBGA	Function	516 PBGA	Function	516 PBGA	Function	516 PBGA	Function	516 PBGA	Function
Y3	I/O<H>	AA19	VCC	AB21	I/O<B>	AC23	PLLOUT<1>	AD25	I/O<B>	AF1	I/O<A>
Y4	I/O<H>	AA20	VCCIO<B>	AB22	GNDPLL<2>	AC24	I/O<B>	AD26	I/O<B>	AF2	I/O<A>
Y5	I/O<H>	AA21	GND	AB23	I/O<B>	AC25	I/O<B>	AE1	GND	AF3	I/O<A>
Y6	VCCIO<H>	AA22	VCCPLL<2>	AB24	I/O<C>	AC26	I/O<C>	AE2	GND	AF4	I/O<A>
Y21	VCCIO<C>	AA23	I/O<C>	AB25	I/O<C>	AD1	I/O<A>	AE3	I/O<A>	AF5	I/O<A>
Y22	I/O<C>	AA24	I/O<C>	AB26	I/O<C>	AD2	PLLOUT<2>	AE4	I/O<A>	AF6	IOCTRL<A>
Y23	I/O<C>	AA25	I/O<C>	AC1	I/O<A>	AD3	PLLRST<3>	AE5	I/O<A>	AF7	I/O<A>
Y24	I/O<C>	AA26	I/O<C>	AC2	I/O<A>	AD4	I/O<A>	AE6	I/O<A>	AF8	I/O<A>
Y25	I/O<C>	AB1	I/O<H>	AC3	I/O<A>	AD5	I/O<A>	AE7	INREF<A>	AF9	I/O<A>
Y26	IOCTRL<C>	AB2	I/O<H>	AC4	I/O<A>	AD6	I/O<A>	AE8	I/O<A>	AF10	I/O<A>
AA1	I/O<H>	AB3	I/O<A>	AC5	I/O<A>	AD7	I/O<A>	AE9	I/O<A>	AF11	I/O<A>
AA2	I/O<H>	AB4	GNDPLL<3>	AC6	I/O<A>	AD8	IOCTRL<A>	AE10	I/O<A>	AF12	CLK<2>/PLLIN<2>
AA3	I/O<H>	AB5	VCCPLL<3>	AC7	I/O<A>	AD9	I/O<A>	AE11	I/O<A>	AF13	I/O<B>
AA4	I/O<A>	AB6	I/O<A>	AC8	I/O<A>	AD10	I/O<A>	AE12	CLK<0>	AF14	I/O<B>
AA5	I/O<A>	AB7	I/O<A>	AC9	I/O<A>	AD11	I/O<A>	AE13	I/O<B>	AF15	I/O<B>
AA6	GND	AB8	I/O<A>	AC10	I/O<A>	AD12	TDI	AE14	I/O<B>	AF16	I/O<B>
AA7	VCCIO<A>	AB9	I/O<A>	AC11	I/O<A>	AD13	CLK<4>DEDCLK/PLLIN<0>	AE15	I/O<B>	AF17	I/O<B>
AA8	VCC	AB10	I/O<A>	AC12	I/O<A>	AD14	I/O<A>	AE16	I/O<B>	AF18	I/O<B>
AA9	VCCIO<A>	AB11	VCC	AC13	I/O<A>	AD15	I/O<B>	AE17	I/O<B>	AF19	IOCTRL<B>
AA10	GND	AB12	I/O<A>	AC14	CLK<1>	AD16	I/O<B>	AE18	I/O<B>	AF20	IOCTRL<B>
AA11	VCC	AB13	I/O<A>	AC15	I/O<B>	AD17	I/O<B>	AE19	I/O<B>	AF21	I/O<B>
AA12	VCCIO<A>	AB14	CLK<3>/PLLIN<1>	AC16	I/O<B>	AD18	INREF<B>	AE20	I/O<B>	AF22	I/O<B>
AA13	GND	AB15	VCC	AC17	I/O<B>	AD19	I/O<B>	AE21	I/O<B>	AF23	I/O<B>
AA14	VCCIO<B>	AB16	I/O<B>	AC18	I/O<B>	AD20	I/O<B>	AE22	I/O<B>	AF24	I/O<B>
AA15	VCC	AB17	I/O<B>	AC19	I/O<B>	AD21	I/O<B>	AE23	I/O<B>	AF25	I/O<B>
AA16	VCC	AB18	I/O<B>	AC20	I/O<B>	AD22	I/O<B>	AE24	I/O<B>	AF26	I/O<B>

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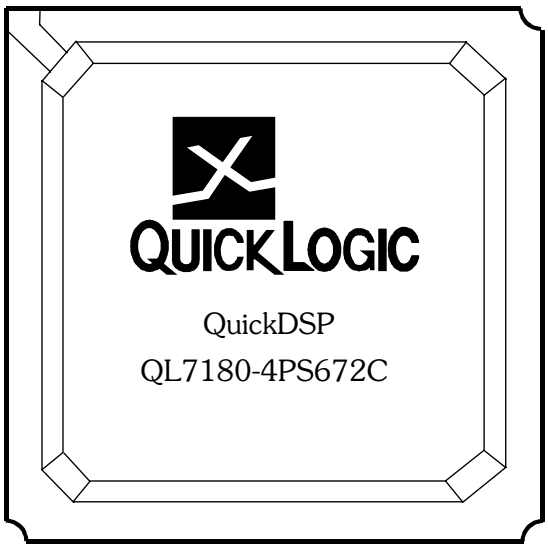
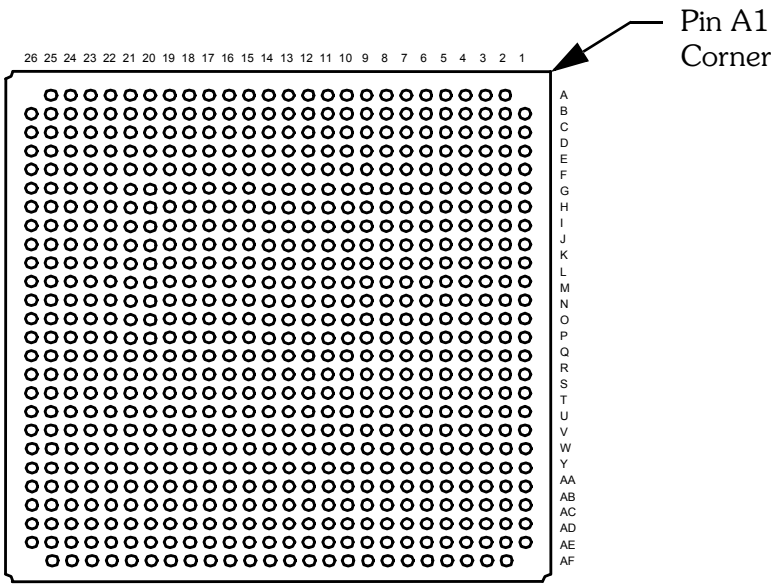
11.0 672 PBGA Pinout Diagram

Top



Bottom



12.0 672 PBGA Pinout Table

Table 19: 672 PBGA Pinout Table

672 PBGA	Function	672 PBGA	Function	672 PBGA	Function	672 PBGA	Function	672 PBGA	Function	672 PBGA	Function
A2	I/O<F>	C10	I/O<F>	E17	I/O<E>	G24	I/O<D>	K5	I/O<G>	M12	GND
A3	I/O<F>	C11	I/O<F>	E18	I/O<E>	G25	I/O<D>	K6	I/O<G>	M13	GND
A4	I/O<F>	C12	I/O<F>	E19	I/O<E>	G26	I/O<D>	K7	I/O<G>	M14	GND
A5	I/O<F>	C13	I/O<F>	E20	I/O<E>	H1	I/O<G>	K8	I/O<G>	M15	GND
A6	I/O<F>	C14	I/O<E>	E21	PLLRST<1>	H2	I/O<G>	K9	I/O<G>	M16	VCC
A7	I/O<F>	C15	I/O<E>	E22	GND	H3	I/O<G>	K10	GND	M17	VCC
A8	I/O<F>	C16	I/O<E>	E23	I/O<E>	H4	I/O<G>	K11	VCC	M18	I/O<D>
A9	I/O<F>	C17	IOCTRL<E>	E24	I/O<E>	H5	I/O<G>	K12	VCC	M19	I/O<D>
A10	I/O<F>	C18	I/O<E>	E25	I/O<D>	H6	I/O<G>	K13	VCC	M20	I/O<D>
A11	I/O<F>	C19	I/O<E>	E26	I/O<D>	H7	VCCIO<G>	K14	GND	M21	I/O<D>
A12	I/O<F>	C20	I/O<E>	F1	I/O<G>	H8	I/O<F>	K15	VCC	M22	I/O<D>
A13	CLK<7>	C21	I/O<E>	F2	I/O<G>	H9	I/O<F>	K16	VCC	M23	I/O<D>
A14	CLK<5>/PLLIN<3>	C22	I/O<E>	F3	I/O<G>	H10	I/O<F>	K17	GND	M24	I/O<D>
A15	I/O<E>	C23	I/O<E>	F4	I/O<F>	H11	I/O<F>	K18	I/O<D>	M25	I/O<D>
A16	I/O<E>	C24	I/O<E>	F5	GND	H12	I/O<F>	K19	I/O<D>	M26	I/O<D>
A17	I/O<E>	C25	I/O<D>	F6	I/O<F>	H13	CLK<8>	K20	I/O<D>	N1	I/O<G>
A18	I/O<E>	C26	I/O<D>	F7	I/O<F>	H14	CLK<6>	K21	I/O<D>	N2	I/O<G>
A19	I/O<E>	D1	IOCTRL<G>	F8	I/O<F>	H15	I/O<E>	K22	I/O<D>	N3	I/O<G>
A20	I/O<E>	D2	I/O<G>	F9	I/O<F>	H16	I/O<E>	K23	I/O<D>	N4	I/O<G>
A21	I/O<E>	D3	I/O<F>	F10	I/O<F>	H17	I/O<E>	K24	I/O<D>	N5	I/O<G>
A22	I/O<E>	D4	I/O<F>	F11	I/O<F>	H18	I/O<E>	K25	I/O<D>	N6	I/O<H>
A23	IOCTRL<E>	D5	I/O<F>	F12	I/O<F>	H19	I/O<E>	K26	I/O<D>	N7	VCCIO<G>
A24	I/O<E>	D6	I/O<F>	F13	I/O<F>	H20	VCCIO<D>	L1	I/O<G>	N8	I/O<G>
A25	I/O<E>	D7	I/O<F>	F14	I/O<E>	H21	I/O<D>	L2	I/O<G>	N9	GND
B1	I/O<G>	D8	I/O<F>	F15	I/O<E>	H22	I/O<D>	L3	I/O<G>	N10	GND
B2	VCCPLL<0>	D9	I/O<F>	F16	I/O<E>	H23	I/O<D>	L4	I/O<G>	N11	GND
B3	I/O<F>	D10	I/O<F>	F17	I/O<E>	H24	I/O<D>	L5	I/O<G>	N12	GND
B4	I/O<F>	D11	I/O<F>	F18	I/O<E>	H25	I/O<D>	L6	I/O<G>	N13	GND
B5	I/O<F>	D12	I/O<F>	F19	I/O<E>	H26	I/O<D>	L7	VCCIO<G>	N14	GND
B6	I/O<F>	D13	I/O<F>	F20	I/O<E>	J1	I/O<G>	L8	I/O<G>	N15	GND
B7	IOCTRL<F>	D14	I/O<E>	F21	GNDPLL<1>	J2	I/O<G>	L9	I/O<G>	N16	VCC
B8	I/O<F>	D15	I/O<E>	F22	PLLOUT<0>	J3	IOCTRL<G>	L10	VCC	N17	VCC
B9	I/O<F>	D16	I/O<E>	F23	I/O<E>	J4	I/O<G>	L11	GND	N18	I/O<D>
B10	I/O<F>	D17	I/O<E>	F24	I/O<D>	J5	I/O<G>	L12	VCC	N19	I/O<D>
B11	I/O<F>	D18	I/O<E>	F25	I/O<D>	J6	I/O<G>	L13	VCC	N20	VCCIO<D>
B12	I/O<F>	D19	I/O<E>	F26	I/O<D>	J7	VCCIO<G>	L14	GND	N21	VCC
B13	TMS	D20	I/O<E>	G1	I/O<G>	J8	GNDPLL<0>	L15	VCC	N22	NC
B14	I/O<E>	D21	I/O<E>	G2	INREF<G>	J9	GND	L16	GND	N23	I/O<D>
B15	I/O<E>	D22	I/O<E>	G3	I/O<G>	J10	I/O<F>	L17	VCC	N24	I/O<D>
B16	I/O<E>	D23	I/O<E>	G4	I/O<G>	J11	I/O<F>	L18	I/O<D>	N25	I/O<D>
B17	I/O<E>	D24	I/O<E>	G5	PLLRST<0>	J12	I/O<F>	L19	I/O<D>	N26	I/O<C>
B18	I/O<E>	D25	I/O<D>	G6	I/O<G>	J13	I/O<F>	L20	VCCIO<D>	P1	I/O<H>
B19	INREF<E>	D26	I/O<D>	G7	I/O<F>	J14	GND	L21	I/O<D>	P2	TCK
B20	I/O<E>	E1	I/O<G>	G8	VCCIO<F>	J15	I/O<E>	L22	I/O<D>	P3	I/O<H>
B21	I/O<E>	E2	I/O<G>	G9	VCCIO<F>	J16	I/O<E>	L23	I/O<D>	P4	I/O<H>
B22	I/O<E>	E3	I/O<F>	G10	I/O<F>	J17	I/O<E>	L24	I/O<D>	P5	VCC
B23	I/O<E>	E4	I/O<F>	G11	VCCIO<F>	J18	GND	L25	I/O<D>	P6	I/O<H>
B24	I/O<E>	E5	I/O<F>	G12	I/O<F>	J19	I/O<E>	L26	I/O<D>	P7	VCCIO<H>
B25	I/O<E>	E6	I/O<F>	G13	VCCIO<F>	J20	VCCIO<D>	M1	I/O<G>	P8	I/O<H>
B26	I/O<D>	E7	I/O<F>	G14	VCCIO<E>	J21	I/O<D>	M2	I/O<G>	P9	I/O<H>
C1	I/O<G>	E8	I/O<F>	G15	I/O<E>	J22	INREF<D>	M3	I/O<G>	P10	VCC
C2	I/O<F>	E9	IOCTRL<F>	G16	VCCIO<E>	J23	IOCTRL<D>	M4	I/O<G>	P11	VCC
C3	PLLOUT<3>	E10	I/O<F>	G17	I/O<E>	J24	IOCTRL<D>	M5	I/O<G>	P12	GND
C4	I/O<F>	E11	I/O<F>	G18	VCCIO<E>	J25	I/O<D>	M6	I/O<G>	P13	GND
C5	I/O<F>	E12	I/O<F>	G19	VCCIO<E>	J26	I/O<D>	M7	I/O<G>	P14	GND
C6	I/O<F>	E13	I/O<F>	G20	VCCPLL<1>	K1	I/O<G>	M8	I/O<G>	P15	GND
C7	I/O<F>	E14	I/O<E>	G21	I/O<E>	K2	I/O<G>	M9	I/O<G>	P16	GND
C8	I/O<F>	E15	I/O<E>	G22	I/O<E>	K3	I/O<G>	M10	VCC	P17	GND
C9	INREF<F>	E16	I/O<E>	G23	I/O<D>	K4	I/O<G>	M11	VCC	P18	GND
P19	I/O<D>	T20	VCCIO<C>	V22	I/O<C>	Y24	I/O<C>	AB26	I/O<C>	AE3	I/O<A>

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Table 19: 672 PBGA Pinout Table (Continued)

672 PBGA	Function	672 PBGA	Function	672 PBGA	Function	672 PBGA	Function	672 PBGA	Function	672 PBGA	Function
P20	VCCIO<C>	T21	I/O<C>	V23	I/O<C>	Y25	I/O<C>	AC2	I/O<H>	AE4	I/O<A>
P21	I/O<C>	T22	I/O<C>	V24	I/O<C>	Y26	I/O<C>	AC3	I/O<A>	AE5	I/O<A>
P22	I/O<C>	T23	I/O<C>	V25	I/O<C>	AA1	I/O<H>	AC4	GND	AE6	I/O<A>
P23	I/O<C>	T24	I/O<C>	V26	I/O<C>	AA2	I/O<H>	AC5	I/O<A>	AE7	INREF<A>
P24	I/O<C>	T25	I/O<C>	W1	I/O<H>	AA3	I/O<H>	AC6	I/O<A>	AE8	I/O<A>
P25	I/O<C>	T26	I/O<C>	W2	INREF<H>	AA4	I/O<A>	AC7	I/O<A>	AE9	I/O<A>
P26	TRSTB	U1	I/O<H>	W3	I/O<H>	AA5	PLLOUT<2>	AC8	I/O<A>	AE10	I/O<A>
R1	I/O<H>	U2	I/O<H>	W4	I/O<H>	AA6	GND	AC9	I/O<A>	AE11	I/O<A>
R2	I/O<H>	U3	IOCTRL<H>	W5	I/O<H>	AA7	VCCPLL<3>	AC10	I/O<A>	AE12	I/O<A>
R3	I/O<H>	U4	I/O<H>	W6	I/O<H>	AA8	I/O<A>	AC11	I/O<A>	AE13	TDI
R4	I/O<H>	U5	I/O<H>	W7	VCCIO<H>	AA9	I/O<A>	AC12	I/O<A>	AE14	CLK<4> DEDCLK/PLLIN<0>
R5	I/O<H>	U6	I/O<H>	W8	I/O<A>	AA10	I/O<A>	AC13	I/O<A>	AE15	I/O<B>
R6	I/O<H>	U7	I/O<H>	W9	I/O<A>	AA11	I/O<A>	AC14	I/O<B>	AE16	I/O<B>
R7	I/O<H>	U8	I/O<A>	W10	I/O<A>	AA12	I/O<A>	AC15	I/O<B>	AE17	I/O<B>
R8	I/O<H>	U9	I/O<A>	W11	I/O<A>	AA13	I/O<A>	AC16	I/O<B>	AE18	I/O<B>
R9	I/O<H>	U10	GND	W12	I/O<A>	AA14	I/O<B>	AC17	I/O<B>	AE19	IOCTRL<B>
R10	VCC	U11	VCC	W13	CLK<1>	AA16	I/O<B>	AC18	I/O<B>	AE20	IOCTRL<B>
R11	VCC	U12	VCC	W14	I/O<B>	AA17	I/O<B>	AC19	I/O<B>	AE21	I/O<B>
R12	GND	U13	GND	W15	I/O<B>	AA18	I/O<B>	AC20	I/O<B>	AE22	I/O<B>
R13	GND	U14	VCC	W16	I/O<B>	AA19	I/O<B>	AC21	I/O<B>	AE23	I/O<B>
R14	GND	U15	VCC	W17	I/O<B>	AA20	I/O<B>	AC22	TDO	AE24	I/O<B>
R15	GND	U16	VCC	W18	I/O<B>	AA21	I/O<B>	AC23	I/O<B>	AE26	I/O<C>
R16	VCC	U17	GND	W19	GNDPLL<2>	AA22	PLLRST<2>	AC24	I/O<B>	AF2	I/O<A>
R17	VCC	U18	I/O<C>	W20	VCCIO<C>	AA23	I/O<B>	AC25	I/O<C>	AF3	I/O<A>
R18	I/O<C>	U19	I/O<C>	W21	I/O<B>	AA24	I/O<C>	AC26	I/O<C>	AF4	IOCTRL<A>
R19	I/O<C>	U20	I/O<C>	W22	I/O<C>	AA25	I/O<C>	AD1	I/O<H>	AF5	I/O<A>
R20	I/O<C>	U21	I/O<C>	W23	I/O<C>	AA26	I/O<C>	AD2	I/O<H>	AF6	I/O<A>
R21	I/O<C>	U22	I/O<C>	W24	I/O<C>	AB1	I/O<H>	AD3	I/O<A>	AF7	I/O<A>
R22	I/O<C>	U23	IOCTRL<C>	W25	IOCTRL<C>	AB2	I/O<H>	AD4	I/O<A>	AF8	I/O<A>
R23	I/O<C>	U24	INREF<C>	W26	I/O<C>	AB3	I/O<A>	AD5	I/O<A>	AF9	I/O<A>
R24	I/O<C>	U25	I/O<C>	Y1	I/O<H>	AB4	I/O<A>	AD6	I/O<A>	AF10	I/O<A>
R25	I/O<C>	U26	I/O<C>	Y2	I/O<H>	AB5	I/O<A>	AD7	I/O<A>	AF11	I/O<A>
R26	I/O<C>	V1	I/O<H>	Y4	I/O<H>	AB6	PLLRST<3>	AD8	I/O<A>	AF12	I/O<A>
T1	I/O<H>	V2	I/O<H>	Y5	I/O<A>	AB7	I/O<A>	AD9	IOCTRL<A>	AF13	CLK<0>
T2	I/O<H>	V3	I/O<H>	Y6	I/O<H>	AB8	I/O<A>	AD10	I/O<A>	AF14	CLK<2>/PLLIN<2>
T3	I/O<H>	V4	I/O<H>	Y7	I/O<A>	AB9	I/O<A>	AD11	I/O<A>	AF15	I/O<B>
T4	I/O<H>	V5	I/O<H>	Y8	VCCIO<A>	AB10	I/O<A>	AD12	I/O<A>	AF16	I/O<B>
T5	I/O<H>	V6	I/O<H>	Y9	VCCIO<A>	AB11	I/O<A>	AD14	I/O<B>	AF17	I/O<B>
T6	I/O<H>	V7	VCCIO<H>	Y10	I/O<A>	AB12	I/O<A>	AD15	I/O<B>	AF18	I/O<B>
T7	VCCIO<H>	V8	GNDPLL<3>	Y11	VCCIO<A>	AB13	I/O<A>	AD16	I/O<B>	AF19	I/O<B>
T8	I/O<H>	V9	GND	Y12	I/O<A>	AB14	CLK<3>/PLLIN<1>	AD17	I/O<B>	AF20	I/O<B>
T9	I/O<A>	V10	I/O<A>	Y13	VCCIO<A>	AB15	I/O<B>	AD18	I/O<B>	AF21	I/O<B>
T10	VCC	V11	I/O<A>	Y14	VCCIO<B>	AB16	I/O<B>	AD19	I/O<B>	AF22	I/O<B>
T11	GND	V12	I/O<A>	Y15	VCC	AB17	I/O<B>	AD20	I/O<B>	AF23	INREF<B>
T12	VCC	V13	GND	Y16	VCCIO<B>	AB18	I/O<B>	AD21	I/O<B>	AF24	I/O<B>
T13	GND	V14	I/O<B>	Y17	I/O<B>	AB19	I/O<B>	AD22	I/O<B>	AF25	I/O<B>
T14	VCC	V15	I/O<B>	Y18	VCCIO<B>	AB20	I/O<B>	AD23	I/O<B>		
T15	GND	V16	I/O<B>	Y19	VCCIO<B>	AB21	PLLOUT<1>	AD24	I/O<B>		
T16	I/O<B>	V18	GND	Y20	I/O<B>	AB22	GND	AD25	I/O<B>		
T17	VCC	V19	I/O<C>	Y21	I/O<B>	AB23	I/O<B>	AD26	I/O<C>		
T18	I/O<C>	V20	VCCIO<C>	Y22	VCCPLL<2>	AB24	I/O<B>	AE1	I/O<H>		
T19	I/O<C>	V21	I/O<C>	Y23	I/O<C>	AB25	I/O<C>	AE2	I/O<A>		

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